(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 889 509 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
07.01.1999 Bulletin 1999/01

(21) Application number: **98111147.9**

(22) Date of filing: **17.06.1998**

(51) Int. Cl.[6]: **H01L 21/322**, H01L 21/18, H01L 21/336, H01L 21/331, H01L 21/332, H01L 21/329, H01L 29/78, H01L 29/739, H01L 29/745, H01L 29/861

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **30.06.1997 US 885878**

(71) Applicant: **HARRIS CORPORATION**
Melbourne Florida 32919 (US)

(72) Inventors:
- **Neilson, John Manning Savidge**
  Norristown, PA 19403 (US)
- **Benjamin, John Lawrence**
  Mountaintop, PA 18707 (US)
- **Zafrani, Maxime**
  Kingston, PA 18704 (US)

(74) Representative:
Meddle, Alan Leonard
FORRESTER & BOEHMERT
Franz-Joseph-Strasse 38
80801 München (DE)

(54) Lifetime control for semiconductor devices

(57) A method of controlling minority carrier lifetime in a semiconductor device in which the density of recombination centers is controlled so that the recombination centers are concentrated in a thin buffer layer adjacent a blocking layer in one of two bonded wafers. The density is controlled by misaligning crystal axes of the two wafers or by doping the bonding surface of one of the wafers before the wafers are bonded. Both methods generate recombination centers in the thin buffer layer that forms around or adjacent the bonding interface. A semiconductor device made by this method includes a buffer layer with a significantly higher density of recombination centers than the adjacent blocking layer.

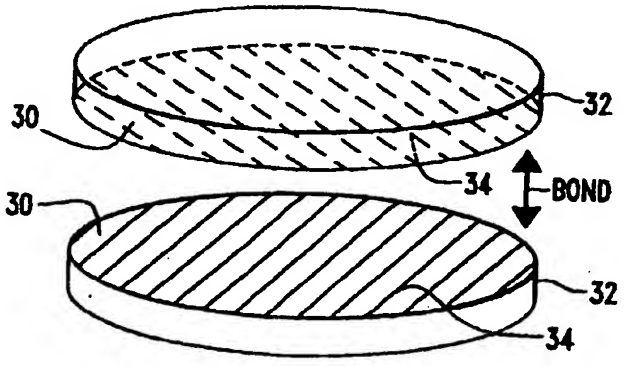

FIG. 3

EP 0 889 509 A2

Description

The present invention is directed to minority carrier lifetime control in semiconductor devices, and more particularly to method and device in which a layer adjacent a blocking layer of a semiconductor device is provided with a significantly higher density of recombination centers.

As is known, the switching speed of semiconductor devices (such as during reverse recovery or turn-off) and the gain of parasitic bipolar transistors in field effect transistors are reduced by reducing the minority carrier lifetime. The minority carrier lifetime is the time to recombination of an electron in a P type semiconductor material or of a hole in an N type semiconductor material. Carrier lifetime is reduced by performing a lifetime control procedure to reduce minority carrier lifetime so that the carriers, the holes and electrons, remaining after conduction will recombine more rapidly. The present invention is directed to an improved lifetime control procedure and to devices fabricated with the procedure.

Carrier lifetime control procedures provide locations, known as recombination centers, in the semiconductor device where recombination of the carriers is facilitated. The recombination centers, whose density may be on the order of 0.1 to 1.5 ppma (parts per million atomic), are locations of crystallographic strain which may be caused by the generation of dislocations in the crystal structure of the silicon, such as by introduction of impurities. Various methods for generating recombination centers are known. For example, silicon may be doped with a heavy metal dopant, such as gold or platinum. The heavy metal dopant (the impurity) generates recombination centers because the heavy metals have energy levels within the forbidden energy band of silicon. A further method of generating recombination centers is to generate dislocations throughout the silicon by bombarding it with radiation, such as high energy electrons, neutrons or protons. The dangling bonds in these dislocations have mid-band energy levels which serve as recombination centers for the carriers. The specification of U.S. Patent No. 4,684,413, discloses the method steps.

It has been found that the recombination centers are concentrated in a thin layer in the semiconductor device adjacent a blocking layer. With reference now to Figures 1a-d which show known semiconductor devices (a rectifier in Figure 1a, a MOSFET in Figure 1b, an IGBT in Figure 1c and an MCT (MOS Controlled Thyristor) in Figure 1d), a semiconductor device may include a substrate 12 with a layer 14 which is more lightly doped and performs various functions depending on the type of device in which it is found. Layer 14 is denoted herein as a blocking layer, although its functions may vary. Blocking layer 14 is atop a relatively more heavily doped layer 16, denoted herein as a buffer layer, which has been found to be the preferred location for a high density of recombination centers.

This preferred location for a high density of recombination centers in a thin layer adjacent blocking layer 14 produces low current leakage, low on-voltage for a given switching speed, and a robust avalanche breakdown. Leakage is lower because recombination centers also are generation centers and generate leakage currents if they are located in blocking layer 14 where they are subjected to the high electric fields which appear in blocking layer 14 when the device is supporting a high voltage. On-voltage is lower for a given speed because carriers in blocking layer 14 are rapidly removed by the electric field which builds as voltage on the device increases, but carriers outside blocking layer 14 are inaccessible to the electric field and must be removed by the slower process of recombination. As a result recombination centers in blocking layer 14 cause a higher on-voltage but are not as effective in improving switching speed as those outside blocking layer 14. Recombination centers in blocking layer 14 may also cause "fragile" breakdown characteristics because they trap some of the majority carriers and so increase the resistivity of the material forming blocking layer 14. When the resistivity of blocking layer 14 is too high, the high field region in avalanche breakdown may become unstable and cause a localized overheating and burnout (denoted a "fragile" breakdown). Reducing the number of recombination centers in blocking layer 14 reduces the likelihood of increasing the resistivity of blocking layer 14 and makes avalanche breakdown more robust, i.e., less "fragile".

One of the problems with the prior art, as is apparent from the distribution of recombination centers (x) in Figures 1a-d, is that the recombination centers are distributed uniformly throughout the silicon crystal, not in the preferred buffer layer adjacent blocking layer 14. Note that, in theory, proton radiation dislocations can be confined to a layer, but this has not been shown to be a practical solution because of the difficulty controlling the very high energy required, on the order of several megavolts.

By way of further background, wafer bonding may be used to fabricate silicon devices. In this process, the bending surfaces of two silicon wafers are polished sufficiently flat so that when the polished surfaces are brought into contact with each other, enough of the neighboring silicon atoms can form covalent bonds across the wafer-to-wafer bonding interface to link the two wafers into a single crystal. The present invention takes advantage of this wafer bonding process to facilitate the formation of the preferred buffer layer which has a significantly higher density of recombination centers than the adjacent blocking layer.

An object of the present invention is to provide a novel method and device in which recombination centers of a semiconductor device are concentrated in a buffer layer at or near a wafer-to-wafer bonding interface, in which the density of recombination centers in a

buffer layer adjacent a blocking layer in a semiconductor device is significantly higher than that of the blocking layer.

Another object is to provide a method and device in which a semiconductor device formed by bonding two wafers has a blocking layer and an adjacent buffer layer containing the wafer-to-wafer bonding interface in which the recombination centers are concentrated in the buffer layer and are substantially absent from the blocking layer, and to provide a method of controlling minority carrier lifetime in a semiconductor device by selectively misaligning features of the bonding surfaces of two wafers to control a density of recombination centers in a layer at or adjacent a wafer-to-wafer bonding interface between the two wafers, the two wafers being bonded so that the features of the bonding surfaces of the two wafers are misaligned to generate dislocations which form the recombination centers in the layer.

The present invention includes a method of controlling minority carrier lifetime in a semiconductor device, comprising the step of: controlling a density of recombination centers at a wafer-to-wafer bonding interface adjacent a blocking layer of the semiconductor device so that the recombination centers are concentrated in a buffer layer adjacent the blocking layer, including bending two wafers at the wafer-to-wafer bonding interface so that features of bonding surfaces of the two wafers at the bonding interface are not aligned, sa as to when bonded, the misaligned features of the two wafers generate dislocations at the bonding interface which form the recombination centers.

The invention also includes a method of controlling minority carrier lifetime in a semiconductor device, comprising the steps of

(a) providing two wafers which are to be bonded at bonding surfaces thereof to form a portion of the semiconductor device;
(b) selectively misaligning features of the bonding surfaces of the two wafers to control a density of recombination centers in a layer adjacent a wafer-to-wafer bonding interface between the two wafers;
(c) bonding the bonding surfaces of the two wafers so that the features of the bonding surfaces of the two wafers are misaligned to generate dislocations which form the recombination centers in the layer, and
(d) doping the bonding surface of at least one of two wafers, thereby generating dislocations at the bending interface which form further recombination centers.

The invention further includes a method of controlling minority carrier lifetime in a semiconductor device, comprising the steps of:

(a) providing two wafers which are to be bonded at bonding surfaces thereof to form a portion of the semiconductor device;
(b) selectively doping at least one of the bonding surfaces of the two wafers to control a density of recombination centers in a layer adjacent a wafer-to-wafer bonding interface between the two wafers, the doping forming the recombination centers in the layer,
(c) bonding the bonding surfaces of the two wafers, and before the doping step, polishing the bonding surfaces of the two wafers, including selecting a dopant for the doping step based on an energy level of the dopant, not its solubility or diffusion coefficient.

The invention will now be described, by way of example, with reference to the accompanying drawings in which;

Figures 1a-d show vertical cross-sections of various semiconductor devices of the prior art illustrating the distribution of recombination centers throughout the silicon substrate.
Figures 2a-d show vertical cross-sections of various semiconductor devices illustrating the layer of recombination centers in embodiments of the present invention.
Figure 3 is a pictorial depiction of two wafers to be bonded illustrating misalignment of crystalline features of the two wafers in an embodiment of the present invention.

Figures 2a-d illustrate semiconductor devices incorporating embodiments of the present invention, a method of controlling minority carrier lifetime in a semiconductor device may include the step of controlling a density of recombination centers (x) at a wafer-to-wafer bonding interface 20 adjacent a blocking layer 22 of the semiconductor device so that the recombination centers are concentrated in a buffer layer 24 at or near bonding interface 20 and adjacent blocking layer 22. Desirably, the density of recombination centers (x) in the buffer layer 24 is in a range of from $10^{14}/cm^3$ to $10^{19}/cm^3$. Also, it is desirable the buffer layer 24 be from 1 micron to 50 microns in thickness. Preferably, the recombination centers (x) are substantially absent from the blocking layer 22 and, typically may be in a concentration of less than the concentration of the buffer layer in the blocking layer 22. The figures show bonding interface 20 inside buffer layer 24, although bonding interface 20 may be at an edge or even slightly spaced from buffer layer 24.

The bonding surface of at least one of two wafers which are to be bonded to form substrate 12 is processed before bonding so that dislocations will form at the wafer-to-wafer bonding interface when the wafers are bonded. The dislocations become recombination centers for the minority carriers. The bonding surface may be processed before bonding by either or both of

the two methods discussed below. As used herein, the term dislocation refers to any strain location regardless of the cause of the strain (e.g., dopant or crystalline misalignment).

Figure 3 illustrates one way to process the bonding surfaces is to purposely misalign corresponding features at the bonding surfaces 30 so that when the two wafers 32 are bonded the features are misaligned thereby creating dislocations at the wafer-to-wafer bonding interface. For example, one of the wafers may be rotated relative to the other so that crystalline axes of the two wafers are not aligned. In Figure 3 these axes are highly exaggerated by the misaligned lines 34 on the facing bonding surfaces 30. By way of further example, one of the bonding surfaces 30 may be polished off-axis relative to the other bonding surface. Lines 34 in Figure 3 are also illustrative of the polishing striations resulting from off-axis polishing. The features of the either of these methods (that is, the crystal axes and the polishing striations) generate dislocations when wafers 32 are bonded. The dislocations are at the wafer-to-wafer bonding interface on both bonding surfaces 30 so that buffer layer 24 is formed with the bonding interface therein.

The amount by which wafers 32 are misaligned determines the dislocation density in buffer layer 24. Desirably, the misalignment between wafers 32 illustrated in Figure 3 is in a range of from one to 45 degrees of the lines 34 of one wafer 32 relative to the other. The greater the misalignment, the higher the density of recombination centers. If desired, the density and distribution of these recombination centers may be modified by appropriate heat treatments, such as a furnace operation or rapid thermal annealing, after bonding.

Another method of controlling the density of recombination centers is to dope one or both of the bonding surfaces with a suitable dopant or dopants. While the dopant chosen typically depends upon the particular application, examples of suitable dopants are, for example, Au, Pt, Pd, Ag, Cu, Fe, Ni, Co. For example, dopants may be evaporated onto or implanted into one or both of the bonding surfaces after polishing and before bonding the two wafers. By way of further example, the lower bonding surface (the one on the wafer which does not have blocking layer 22 therein) may be doped with a suitable metal dopant prior to polishing and bonding, and using conventional high temperature treatments to distribute the dopants in what will become buffer layer 24 and establish the desired concentration. Desirably, the dopant concentration in the buffer layer 24 is in a range from $10^{14}/cm^3$ to $10^{19}/cm^3$, depending on the speed required. These doping methods may be used with the wafers aligned, or with the wafers purposely misaligned by a controlled amount to provide a combination of sources of recombination centers.

One of the advantages of the dopant method is that the dopant may be selected to provide optimum switching performance (if this is desired) without regard for its solubility or diffusion coefficient. In prior art lifetime control doping (albeit not at the bonding interface which is unique to the present invention) the dopant was typically a heavy metal evaporated on to one surface of the wafer which was then heated to 800° to 900°C at which the solid solubility of the metal produced an appropriate concentration of recombination centers. The metal had to have an appropriately high diffusion rate so that it could diffuse into the wafer in an acceptable time at this temperature. Gold and platinum were typically used because they provided the appropriate combination of energy level, solid solubility and diffusion coefficient to allow the prior art processes to work. Other metals did not meet the needed combination of characteristics. In contrast, in the present invention when the dopant is applied just prior to bonding, almost any dopant can be used and may be chosen based on energy level alone.

The dopants do not move far from the wafer-to-wafer bonding interface because the subsequent bonding temperatures are low enough to not cause any appreciable diffusion. Of course, if some controlled amount of diffusion of the dopants is desired, suitable heat treatments may be used.

References to bonding herein are intended to refer generally to any conventional bonding technique, and particularly to the above-mentioned wafer bonding method in which the bonding surfaces of two silicon wafers are polished sufficiently flat so that when the polished surfaces are brought into contact with each other, enough of the neighboring silicon atoms can form covalent bonds across the wafer-to-wafer bonding interface to link the two wafers into a single crystal.

A method of controlling minority carrier lifetime in a semiconductor device in which the density of recombination centers is controlled so that the recombination centers are concentrated in a thin buffer layer adjacent a blocking layer in one of two bonded wafers. The density is controlled by misaligning crystal axes of the two wafers or by doping the bonding surface of one of the wafers before the wafers are bonded. Both methods generate recombination centers in the thin buffer layer that forms around or adjacent the bonding interface. A semiconductor device made by this method includes a buffer layer with a significantly higher density of recombination centers than the adjacent blocking layer.

The features disclosed in the foregoing description in the following claims and/or in the accompanying drawings may, both separately and in combination thereof, be material for realising the invention in diverse forms thereof.

Claims

1. A method of controlling minority carrier lifetime in a semiconductor device, comprising the step of: controlling a density of recombination centers at a wafer-to-wafer bonding interface adjacent a blocking layer of the semiconductor device so that the

recombination centers are concentrated in a buffer layer adjacent the blocking layer, including bonding two wafers at the wafer-to-wafer bonding interface so that features of bonding surfaces of the two wafers at the bonding interface are not aligned, sa as to when bonded, the maligned features of the two wafers generate dislocations at the bonding interface which form the recombination centers.

2. A method as claimed in claim 1 including the step of setting a desired density of the recombination centers by selection of a degree of misalignment of the bonding surface features of the two wafers, and polishing the bonding surface of one of the two wafers at a different angle than the features of the bonding surface of the other of the two wafers.

3. A method as claimed in claim 2 including rotating one of the two wafers relative to the other of the two wafers to misalign their bonding surface features, and doping a bonding surface of at least one of two wafers which are to be bonded at the wafer-to-wafer bonding interface, so as form the recombination centers.

4. A method as claimed in claim 3 including the steps of before the doping step, polishing the bonding surfaces of the two wafers; and after the doping step, bonding the polished bonding surfaces of the two wafers.

5. A method as claimed in claims 3 or 4, wherein the doping step comprises the step of evaporating a dopant onto the bonding surface.

6. A method as claimed in any one of claims 1 to 5, wherein the doping step comprises the step of implanting a dopant into the bonding surface, in which the doping step comprises the steps of: doping with a metal dopant one of the two wafers which does not contain the blocking layer, and heating to distribute the metal dopant.

7. A method as claimed in claim 6 intruding the step of bonding the two wafers so that features of the bonding surfaces of the two wafers are not aligned, whereby, when bonded, the misalignment of the two wafers generates dislocations at the bonding interface which form further recombination centers, and the bonding of the two wafers so that features of the bonding surfaces of the two wafers are aligned, thereby avoiding formation of further recombination centers caused by misalignment of the two wafers.

8. A method as claimed in any one of claims 3 to 6 including the step of selecting a dopant for the doping step based on an energy level of the dopant, not on its solubility or diffusion coefficient, preferably in which a dopant for the doping step is one of Au, Pt, Pd, Ag, Cu, Fe, Ni, and Co.

9. A method as claimed in claim 8 wherein the concentration of a dopant in the buffer layer is in a range of from $10^{14}/cm^3$ to $10^{19}/cm^3$, and the density of the recombination centers concentrated in the buffer layer is in a range of from $10^{14}/cm^3$ to $10^{19}/cm^3$, and the thickness of the buffer layer is in a range of from 1 micron to 50 microns.

10. A method as claimed in claim 9, wherein the density of the recombination centers concentrated in the buffer layer is in a range of from $10^{14}/cm^3$ to $10^{19}/cm^3$.

11. A method of controlling minority carrier lifetime in a semiconductor device, comprising the steps of

(a) providing two wafers which are to be bonded at bonding surfaces thereof to form a portion of the semiconductor device;
(b) selectively misaligning features of the bonding surfaces of the two wafers to control a density of recombination centers in a layer adjacent a wafer-to-wafer bonding interface between the two wafers;
(c) bonding the bonding surfaces of the two wafers so that the features of the bonding surfaces of the two wafers are misaligned to generate dislocations which form the recombination centers in the layer, and
(d) doping the bonding surface of at least one of two wafers, thereby generating dislocations at the bonding interface which form further recombination centers.

12. A method as claimed in claim 11 wherein the step of selectively misaligning features of the bonding surfaces of the two wafers provides a degree of misalignment of the features of one of the two wafers relative to the other in a range of from one to 45 degrees.

13. A method of controlling minority carrier lifetime in a semiconductor device, comprising the steps of:

(a) providing two wafers which are to be bonded at bonding surfaces thereof to form a portion of the semiconductor device;
(b) selectively doping at least one of the bonding surfaces of the two wafers to control a density of recombination centers in a layer adjacent a wafer-to-wafer bonding interface between the two wafers, the doping forming the recombination centers in the layer,
(c) bonding the bonding surfaces of the two

wafers, and before the doping step, polishing the bonding surfaces of the two wafers, including selecting a dopant for the doping step based on an energy level of the dopant, not its solubility or diffusion coefficient.

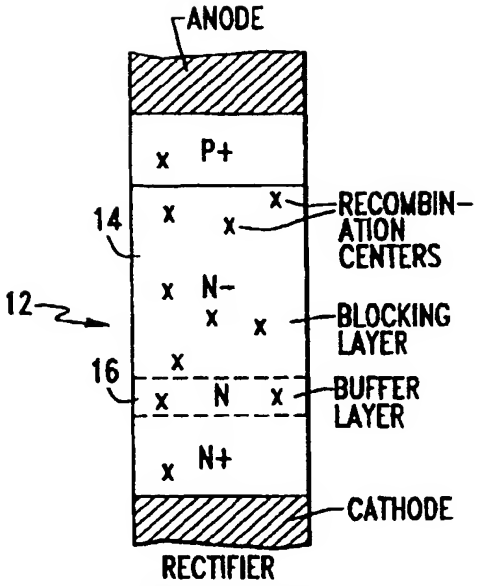

FIG. 1a
PRIOR ART

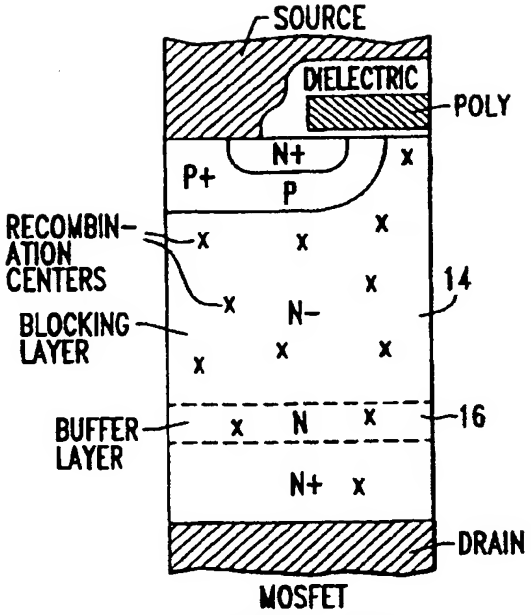

FIG. 1b
PRIOR ART

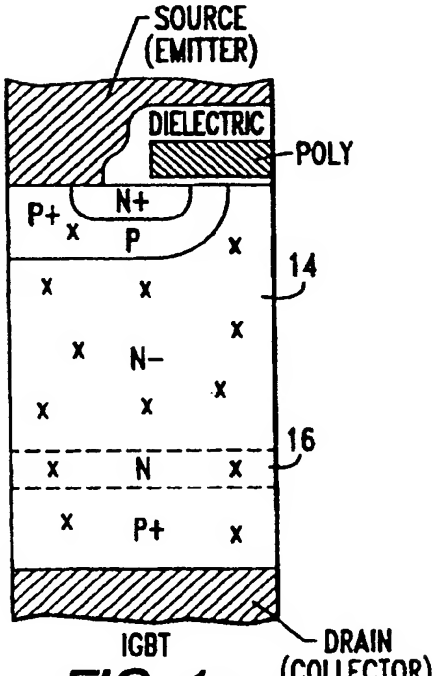

FIG. 1c
PRIOR ART

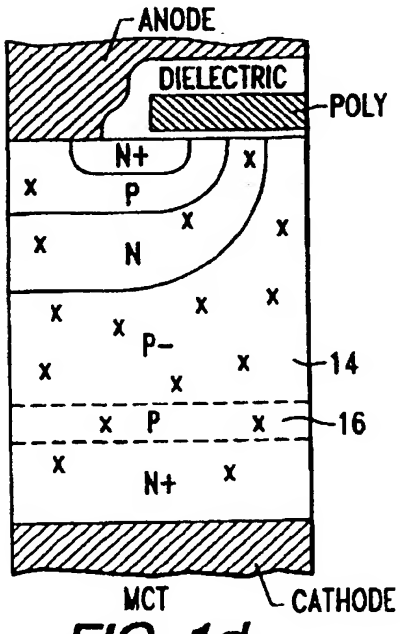

FIG. 1d
PRIOR ART

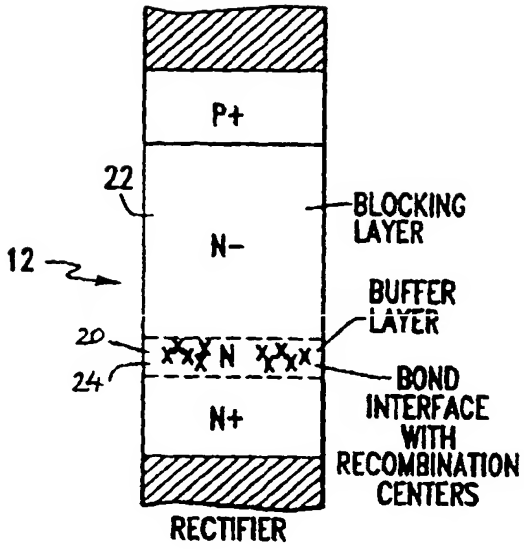

FIG. 2a

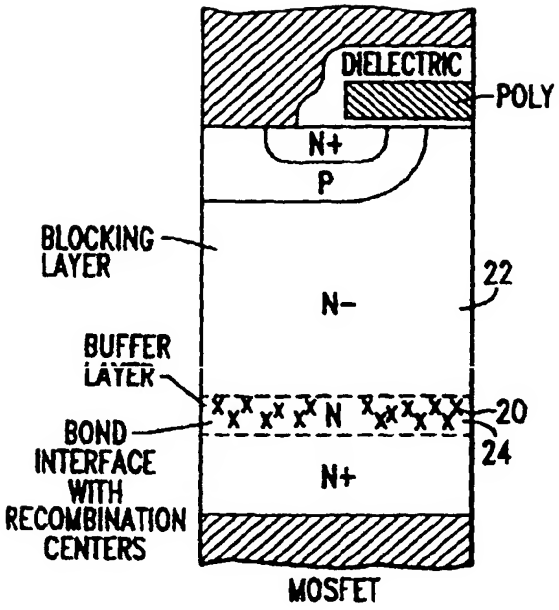

FIG. 2b

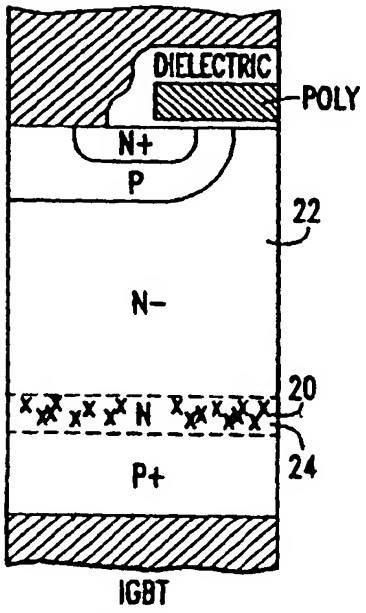

FIG. 2c

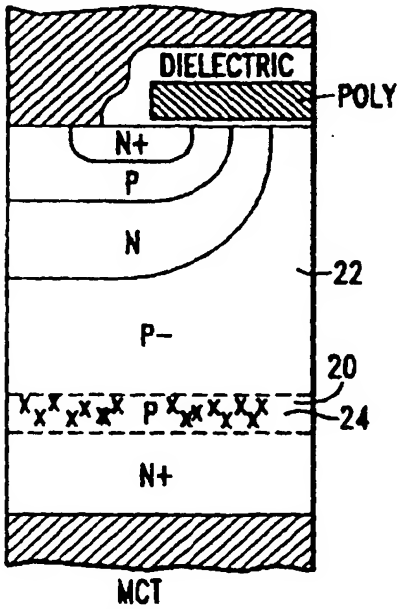

FIG. 2d

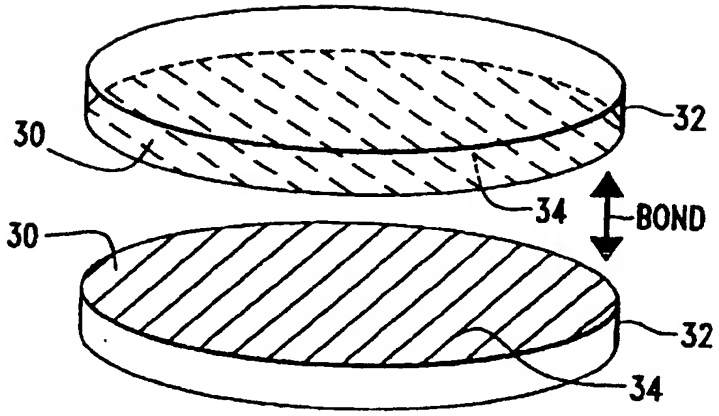

FIG. 3

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 889 509 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
17.11.1999 Bulletin 1999/46

(43) Date of publication A2:
07.01.1999 Bulletin 1999/01

(21) Application number: **98111147.9**

(22) Date of filing: **17.06.1998**

(51) Int. Cl.[6]: **H01L 21/322**, H01L 21/18, H01L 21/336, H01L 21/331, H01L 21/332, H01L 21/329, H01L 29/78, H01L 29/739, H01L 29/745, H01L 29/861

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **30.06.1997 US 885878**

(71) Applicant: **HARRIS CORPORATION**
Melbourne Florida 32919 (US)

(72) Inventors:
- **Neilson, John Manning Savidge**
  Norristown, PA 19403 (US)
- **Benjamin, John Lawrence**
  Mountaintop, PA 18707 (US)
- **Zafrani, Maxime**
  Kingston, PA 18704 (US)

(74) Representative:
Meddle, Alan Leonard
FORRESTER & BOEHMERT
Franz-Joseph-Strasse 38
80801 München (DE)

(54) Lifetime control for semiconductor devices

(57) A method of controlling minority carrier lifetime in a semiconductor device in which the density of recombination centers is controlled so that the recombination centers are concentrated in a thin buffer layer adjacent a blocking layer in one of two bonded wafers. The density is controlled by misaligning crystal axes of the two wafers or by doping the bonding surface of one of the wafers before the wafers are bonded. Both methods generate recombination centers in the thin buffer layer that forms around or adjacent the bonding interface. A semiconductor device made by this method includes a buffer layer with a significantly higher density of recombination centers than the adjacent blocking layer.

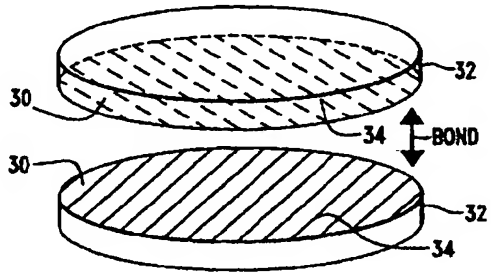

FIG. 3

EP 0 889 509 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 11 1147

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y A	WO 92 09099 A (BOSCH GMBH ROBERT) 29 May 1992 (1992-05-29) * page 15, line 32 - page 19, line 31 * * figures 6,10,11 * * claims 4,6,8 *	1,2,11, 12 6,8-10 3,5,7	H01L21/322 H01L21/18 H01L21/336 H01L21/331 H01L21/332 H01L21/329 H01L29/78 H01L29/739 H01L29/745 H01L29/861
Y	CATANIA M F ET AL: "OPTIMIZATION OF THE TRADEOFF BETWEEN SWITCHING SPEED OF THE INTERNAL DIODE AND ON-RESISTANCE IN GOLD- AND PLATINUM-IMPLANTED POWER METAL-OXIDE-SEMICONDUCTOR DEVICES" IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 39, no. 12, 1 December 1992 (1992-12-01), pages 2745-2749, XP000323175 * paragraphs [00II]-[0III] *	6,8-10	
A	EP 0 327 316 A (TOKYO SHIBAURA ELECTRIC CO) 9 August 1989 (1989-08-09) * column 3, line 36 - line 61 * * figures 2B-2E *	4	
A	US 4 203 780 A (HAYASHI HISAO ET AL) 20 May 1980 (1980-05-20) * abstract * * column 1, line 36 - line 56 *	8-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
D,A	US 4 684 413 A (GOODMAN ALVIN M ET AL) 4 August 1987 (1987-08-04) *the whole document *	1-12	

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
BERLIN	14 April 1999	Polesello, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

Application Number
EP 98 11 1147

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

1-12

European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 98 11 1147

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-12

   Method of bonding two substrates with misaligned features

2. Claim : 13

   Method of polishing, doping and then bonding two substrates

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 98 11 1147

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-04-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9209099 A	29-05-1992	DE 4036222 A	21-05-1992
		DE 59108592 D	10-04-1997
		EP 0557318 A	01-09-1993
		JP 6502277 T	10-03-1994
EP 0327316 A	09-08-1989	JP 1199469 A	10-08-1989
		JP 2070752 C	10-07-1996
		JP 7107935 B	15-11-1995
		DE 68911702 D	10-02-1994
		DE 68911702 T	28-04-1994
		US 5023696 A	11-06-1991
US 4203780 A	20-05-1980	DE 2838545 A	20-03-1980
		GB 2028580 A,B	05-03-1980
US 4684413 A	04-08-1987	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82